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**GOVERNMENT POLYTECHNIC, NANDED**

**MICRO PROJECT**

**Academic year: 2019-20**

**TITLE OF THE PROJECT**

Output of AND Logic Gates.

**Program: Information Tech. Program code: IF3I**

**Course: DTM Course code: 22323**

**Name of Guide:- S.R. SHAMRAJ**

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This is certifying that **Roll No.** **945,948,949** of **3rd** Semester of Diploma in **Information Technology** of Institute, GOVERNMENT POLYTECHNIC has completed the Micro Project satisfactorily in Subject -**DTM (22323)** for the academic year **2019- 2020** as prescribed in the curriculum.

Place: **Nanded**

Date: ………………………

**Subject Teacher Head of the Department Principal**

S.R. SHAMRAJ S.N.DHOLE DR.G.V.GARJE

**WEEKLY PROGRESS REPORT**

**TITLE OF THE MICRO PROJECT:- Output of AND Logic Gates**

|  |  |  |  |
| --- | --- | --- | --- |
| **WEEK** | **ACTIVITY PERFORMED** | **SIGN OF GUIDE** | **DATE** |
| **1ST** | **Discussion and finalization of Topic** |  |  |
| **2ND** | **Discussion and finalization of Topic** |  |  |
| **3RD** | **Preparation and submission of Abstract** |  |  |
| **4TH** | **Literature Review** |  |  |
| **5TH** | **Collection of Data** |  |  |
| **6TH** | **Collection of Data** |  |  |
| **7TH** | **Collection of Data** |  |  |
| **8TH** | **Collection of Data** |  |  |
| **9TH** | **Discussion and Outline of Content** |  |  |
| **10TH** | **Formulation of Content** |  |  |
| **11TH** | **Editing and 1st Proof Reading of Content** |  |  |
| **12TH** | **Editing and 2nd Proof Reading of Content** |  |  |
| **13TH** | **Compilation of Report and Presentation** |  |  |
| **14TH** | **Seminar** |  |  |
| **15TH** | **Viva-voce** |  |  |
| **16TH** | **Final submission of Micro project** |  |  |

**Sign of the student Sign of the faculty**

**S.R. SHAMRAJ**

**ANEEXURE II**

**Evaluation Sheet for the Micro Project**

**Academic Year: 2019-20 Name of the Faculty: S.R. SHAMRAJ**

**Course: DTM Course code: 22323 Semester: III**

**Title of the project: Output of AND Logic Gates**

**Cos addressed by Micro Project:**

**A:** Formulate grammatically correct sentences.

**B:** Give presentation by using audio visual aids.

**C:** Communicate Skillfully.

**D:** Write reports using correct guidelines.

**Major learning outcomes achieved by students by doing the project**

1. **Practical outcome:**
2. Deliver presentation (seminar) effectively.
3. **Unit outcomes in Cognitive domain:**
4. Prepare the points for computer presentation.
5. Make seminar presentation.
6. **Outcomes in Affective domain:**
7. Function as team member.
8. Follow Ethics.
9. Make proper use of computer and Internet

**Comments/suggestions about team work /leadership/inter-personal communication (if any)**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Roll No** | **Student Name** | **Marks out of 4 for performance in group activity**  **(D5 Col.8)** | **Marks out of 2for performance in oral/ presentation**  **(D5 Col.9)** | **Total out of 06** |
| **945** | **Harsh santosh zanwar** |  |  |  |
| **948** | **Amaan Khan Pathan** |  |  |  |
| **949** | **MD .Hifaz Ali Khan** |  |  |  |

**(Signature of Faculty)**

**S.R. SHAMRAJ**

**Group Details**

|  |  |  |
| --- | --- | --- |
| **Roll No.** | **Name** | **Enrollment No.** |
| 945 | Harsh Santosh Zanwar | 1800200119 |
| 948 | Amaan khan Pathan | 1815660 |
| 949 | MD.Hifaz khan | 1815660141 |

**Course :** Digital technique and Microprocessor

**Name of Guide:** S.R. SHAMRAJ

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| **4** | **AND Gate Information** | **3** |
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**Introduction**

In electronics, Logic gates are the building blocks of every electronic circuit. Logic gates defined as the simple electronic circuits having one or more input and a single output. Their operation varies from one type of logic gate to another. The relationship between input and output follow a certain logical equation.

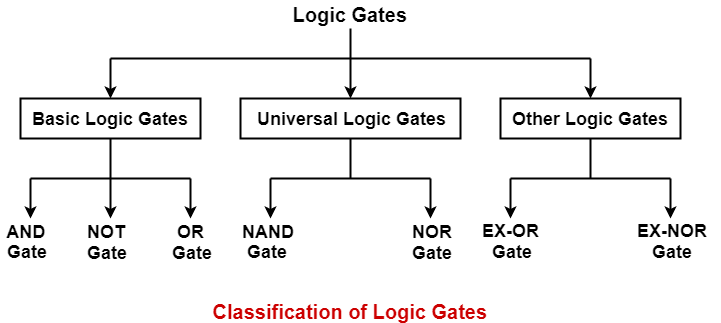
Basically, all logic gates have one output and two inputs. Some logic gates like NOT gate or Inverter has only one input and one output. The inputs of the logic gates are designed to receive only binary data (only low 0 or high 1) by receiving the voltage input. The low logic level represents Zero volts and high logic level represents 3- or 5-volts positive supply voltage. We can connect any number of logic gates to design a required digital circuit. Practically, we implement the large number of logic gates in ICs, by which we can save the physical space occupied by the large number of logic gates. We can also perform complicated operations at high speeds by using integrated circuits (IC).By combining logic gates, we can design many specific circuits like flip flops, latches, multiplexers, shift registers etc.

Logic Gates

In electronics, Logic gates are the building blocks of every electronic circuit. Logic gates defined as the simple electronic circuits having one or more input and a single output. Their operation varies from one type of logic gate to another. The relationship between input and output follow a certain logical equation

**Types of Logic Gates-**

**Logic gates can be broadly classified as-**



## ****Basic Logic Gates-****

**Basic Logic Gates are the fundamental logic gates using which universal logic gates and other logic gates are constructed.**

## ****Properties of Basic Logic Gates-****

* Basic logic gates are associative in nature.
* Basic logic gates are commutative in nature.

## ****Types of Basic Logic Gates**-**

In digital electronics, there are mainly three basic logic gates which are-

1. AND Gate
2. OR Gate
3. NOT Gate

## ****1. AND Gate-****

* The output of AND gate is high (‘1’) if all its inputs are high (‘1’).
* The output of AND gate is low (‘0’) if any one of its inputs is low (‘0’)

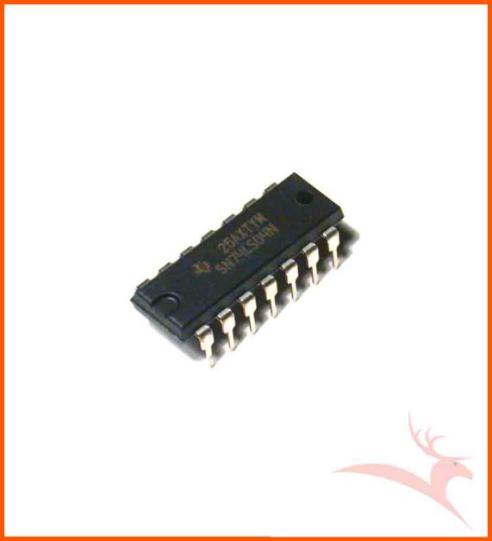
**2. OR Gate-**

* The output of OR gate is high (‘1’) if any one of its inputs is high (‘1’).
* The output of OR gate is low (‘0’) if all its inputs are low (‘0’).

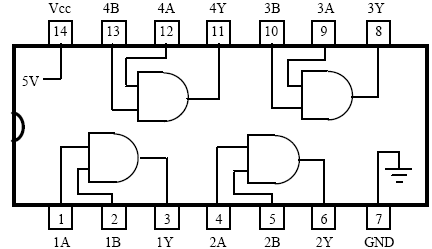
3. **NOT Gate-**

* The output of NOT gate is high (‘1’) if its input is low (‘0’).
* The output of NOT gate is low (‘0’) if its input is high (‘1’).
* AND Logic gates

|  |  |  |
| --- | --- | --- |
| **INPUT** | | **OUTPUT** |
| A | B | A AND B |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |



**AND GATE IC 7408**



**Reference**

1)[AND](https://en.wikipedia.org/wiki/AND_gate" \t "_blank)**[gate](https://en.wikipedia.org/wiki/AND_gate" \t "_blank)**[- Wikipedia](https://en.wikipedia.org/wiki/AND_gate" \t "_blank)https://en.wikipedia.org/wiki/AND\_gate

### **[2)Logical AND Gate | Electrical4U](2)Logical AND Gate | Electrical4Uhttps://www.electrical4u.com/logical-and-gate/)**

[https://www.electrical4u.com/logical-and-gate/](2)Logical AND Gate | Electrical4Uhttps://www.electrical4u.com/logical-and-gate/)

3)Manual

**4)Tech-Max Book**

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**Subject Teacher Head of the Department Principal**

S.R. SHAMRAJ S.N.DHOLE DR.G.V.GARJE

**CONCLUSION**

**REFERENCE:**

**SOURCES USED**